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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,073	03/11/2004	Chul Ho Ham	MRE-0070	4384

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

N/A

Office Action Summary	Application No.	Applicant(s)	
	10/797,073	HAM ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-5 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the test socket". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto et al. ("Yamamoto") USPN 6,267,603.

Yamamoto discloses in figs. 1-10 a carrier module comprising: a carrier module body for seating a semiconductor device on an underside thereof, having a pass through hole 23 (fig. 1) from an upper part to the underside the semiconductor device 24 is seated thereon; a housing 3 over the carrier module body; a supplementary housing 4 fitted in a lower part of the housing to be movable in up/down directions (col. 5, lines 53-55), for elastic contact with the carrier module body by a first elastic member 26 fitted inside of the housing; a vacuum tube 13 in the supplementary housing so as to be in communication with the pass through hole in the carrier module body; at least one pair of latches 34 in a lower part of the carrier module body to move apart or close in an outer or inner side, for holding or releasing the semiconductor device seated on the carrier module body (col. 6, lines 46-62); a latch button 28/37 fitted in an upper part of the carrier module body so as to be movable in up/down directions, and coupled to the latch with a connection pin 36 for moving in up/down directions by an external force, to making the latch to move; and a second elastic member 26/35 for elastic supporting of the latch buttons on the carrier module body, thereby, when the semiconductor device is brought into contact with the test socket, and tested, holding the semiconductor device with a vacuum 31 formed through the pass through hole in the carrier module body and the vacuum tube in a state the latch releases the semiconductor device (col. , lines 60-64).

Regarding claim 5, Yamamoto discloses (col. 7, lines 41-57) a latch pusher 34a projected upward from one side part of the test socket to be brought into contact with the semiconductor

device, and a projection 30 projected outwardly from an outer part of the latch, for being brought into contact with the latch pusher.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kerdiya et al. ("Kerdiya") USPN 5,491,419 in view of Sano et al. ("Sano") US PG-Pub 2003/0054676.

Kerdiya discloses (fig. 2-5 and col. 7, lines 45-53) a carrier module comprising: a carrier module body for seating a semiconductor device on an underside thereof, having a pass through hole from an upper part to the underside the semiconductor device is seated thereon; a housing 25 over the carrier module body; a supplementary housing 26 fitted in a lower part of the housing to be movable in up/down directions (col. 4, lines 49-55), for elastic contact with the carrier module body by a first elastic member 32 fitted inside of the housing; a vacuum tube 27 in the supplementary housing so as to be in communication with the pass through hole in the carrier module body; and a second elastic member 36, but lacks anticipation of a latch.

Sano discloses in figs. 2-4 a carrier module comprising: a carrier module body for seating a semiconductor device at least one pair of latches 21 in a lower part of the carrier module body to move apart or close in an outer or inner side, for holding or releasing the semiconductor device seated on the carrier module body; a latch button 21b fitted in an upper part of the carrier module body so as to be movable in up/down directions, and coupled to the latch with a

connection pin 14 (par. 0052) for moving in up/down directions by an external force, to making the latch to move; an elastic member 12 for elastic supporting of the latch buttons on the carrier module body, thereby, when the semiconductor device is brought into contact with the test socket, and tested, holding the semiconductor device with a vacuum formed through the pass through hole in the carrier module body and the vacuum tube in a state the latch releases the semiconductor device (pars. 0046-0048).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Sano's teachings with Kerdiya's device since that would eliminate the need for any slits as taught by Sano.

Regarding claim 3, Kerdiya discloses an O-ring 44 fitted at a connection of the supplementary housing and the carrier module.

Regarding claim 4, Sano discloses a latch 21 having a slanted slot of a long hole form for inserting a guide pin 15 therein, wherein the latch is opened or closed, as the slanted slot slides along the guide pin.

Regarding claim 5, Sano discloses a latch pusher 21a projected upward from one side part of the test socket to be brought into contact with the semiconductor device; and a projection 11 projected outwardly from an outer part of the latch, for being brought into contact with the latch pusher.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Sano et al. JP 2003-86319 ("Sano '319").

Yamamoto discloses the device structure as recited in the claim, but lacks anticipation of a slanted slot of a long hole form.

Sano '319 discloses in figs. 2-4 a carrier module comprising: a carrier module body for seating a semiconductor device on an underside thereof; and a latch 21 having a slanted slot of a long hole form for inserting a guide pin 15 therein, wherein the latch is opened or closed, as the slanted slot slides along the guide pin.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Sano '319's teachings with Yamamoto's device since that would eliminate the need for any molding techniques as taught by Sano '319.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamto/Kerdiya in view of Sano as applied to claim 1 above, and further in view of Elder et al. ("Elder") USPN 5,123,850.

The combined references disclose the device structure as recited in the claim, but lack anticipation of a heat sink.

Elder discloses in figs. 1-7 a module comprising: a carrier module body for seating a semiconductor device on an underside thereof; and a heat sink 23 in a central part of the body, for bringing into contact with a surface of the semiconductor device, and transferring heat.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Elder's teachings with Yamamoto's device since that would provide an efficient heat transfer system as taught by Elder.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
February 16, 2005

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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